



10-, 12-, OR 14-BIT SYNCHRO-TO-DIGITAL/ RESOLVER-TO-DIGITAL CONVERTER

LOWER COST! PIN-FOR-PIN REPLACEMENT FOR SDC-630/632/634 SERIES. FOR ALL NEW DESIGNS!

DESCRIPTION

APPLICATIONS

The SDC-630/632/634 A/ST series are low cost, low profile synchro-todigital (S/D) and resolver-to-digital (R/D) tracking converters with standard pin configurations. They use a unique control transformer algorithm that provides inherently higher accuracy and jitter-free output. Utilizing a type II servo loop, these converters have no velocity lag up to the specified tracking rate, and output data is always fresh and continuously available. Each unit is fully trimmed and requires no adjustment or field calibration. These converters may be used wherever analog angle data from a synchro or resolver must be rapidly and accurately converted to digital form for transmission, storage or analysis. Because these units are extremely rugged and stable, and meet the requirements on MIL-STD-202E, they are suitable for the most severe industrial, commercial and military applications. Military ground support and avionics uses include ordnance control, radar tracking systems, navigation and collision avoidance systems.

FEATURES

- Low Cost Pin-for-Pin Replacement for SDC-630/632/634 Series
- Industry Standard Low Profile
 Modular Converters
- Accuracy: 10 Bit: 21 Minutes 12 Bit: 8.5 Minutes 14 Bit: 4 Minutes, 0.9 LSB or 2.6 Minutes (High Accuracy)
- Options (Consult Factory): Velocity Input BIT: Built-In-Test 16-Bit Resolution

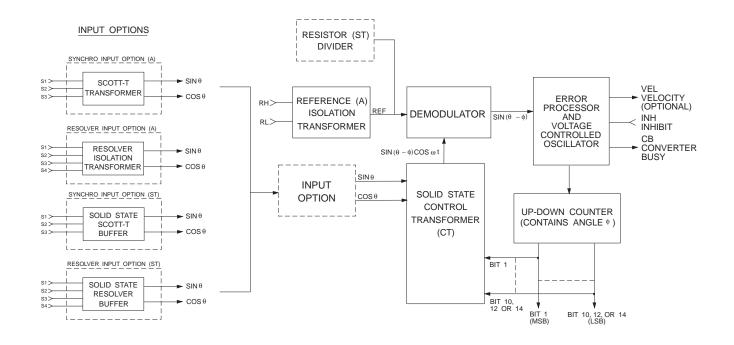


FIGURE 1. SDC-630/632/634 A/ST BLOCK DIAGRAM

PARAMETER VALUE						
	SDC-630	SDC-632				
RESOLUTION	10 bits	12 bits	14 bits			
ACCURACY						
Standard Units High Accuracy Option	±21 min _	±8.5 min _	±5.3 min ±2.6 min			
SIGNAL AND REFERENCE INPUT	Signal Frequency Range	Imp	nal Input edance ced, Resistive)			
		A*	ST			
Synchro Input 90V L-L, 400 Hz (Option H)	350-1000 Hz	148 kΩ min	123 k			
90V L-L, 60 Hz (Option I)	47-1000 Hz	148 k Ω min	123 k			
11.8V L-L, 400 Hz (Option L) Resolver Input	350-1000 Hz	19 kΩ min	52 k			
90V L-L, 400 Hz	350-1000 Hz	148 k Ω min				
(Option H) 26V L-L, 60 Hz (Option M)	350-1000 Hz	42 k Ω min				
(Option M) 11.8V L-L, 400 Hz (Option L)	350-1000 Hz	19 kΩ min	70 k			
REFERENCE INPUT	Reference Voltage Range	Reference Input Impedance (Resistive)				
Options H, I Options M, L	40-150 Vrms 10- 50 Vrms	300 kΩ min 80 kΩ min	270 k 60 k			
* Transformer Isolated. C special order.	other voltages a	nd frequencie	s available on			
DIGITAL INPUT/OUTPUTS Logic Type Inhibit Input (INH) Outputs Type 10, 12, 14, (For 16 Consult Factory) Parallel Data Bits Converter Busy (CB) Drive Capability Built-In-Test (BIT) (Special Order,	TTL/CMOS Compatible Logic "0" inhibits Does not interrupt converter tracking. TTL/CMOS Natural Binary Angle; Positive logic 0.5 to 1.5 μsec positive pulse. Data changes on leading edge. 1 Std. TTL load					
Consult Factory) VELOCITY OUTPUT (SPECIAL ORDER) Polarity	Positive Outpu	It for increasin	g angle			
Std. Voltage Range (Full Scale)	±4 Min (Other ranges available; Consult Factory)					
For other Velocity Characteristics Consult Factory						

PARAMETER	VALUE					
POWER SUPPLIES	+15 V Supply	-15 V Supply	+ 5 V Supply			
Nominal Voltage Range Maximum Voltage Without Damage Current (All)	+11 to +16.5 V +18 V 20 mA	-11 to -16.5 V -18 V 25 mA	+4.5 to +5.5 V +7 10 mA			
TEMPERATURE RANGES Operating -1 Option -3 Option Storage	-55°C to +105°C 0°C to +70°C -55°C to +125°C					
PHYSICAL CHARACTERISTICS Size (Encapsulated Module) Weight		x 2.625 x 0.43 i x 6.67 x 1.07 4 oz. (113 gm.)				

signal amplitude variation, and reference input.

POWER SUPPLIES

The main power supplies can vary over the specified ranges with no change in converter specifications, except for a proportional change in maximum tracking rates.

When testing or evaluating the converters, it is advisable to limit the current in each of the supplies. Set each current limit 50% greater than the maximum current listed for that supply as listed in TABLE 1.

TIMING

FIGURE 2 shows the converter timing waveforms. Whenever an input angle change occurs, the converter changes the digital angle in 1 LSB steps, and generates a Converter Busy (CB) pulse. The CB is a positive pulse 0.5 to 1.5 µsec long.

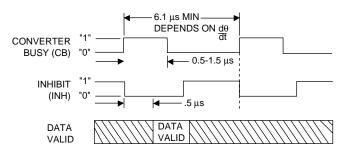


FIGURE 2. SDC-630/632/634* A/ST TIMING DIAGRAM

Bandwidth (non F carrier)		60 HZ			400 HZ				UNITS
Carrier Frequency Range Bandwidth (Closed Loop)		47 - 1,000 15				360 - 1,000 (ST to 5,000) 100			
Ka A1 A2 A		1,100 0.1 7,600 33 16.3 10 12 14 16			48,000 1 48,000 220 110 10 12 14 16				1/s 1/s 1/s 1/s 1/s UNITS
B RESOLUTION	10								
Tracking Rate (rps) Typical Minimum Acceleration (1 LSB lag) Settling Time (179° step, max)	28.5 24 370 500	7.1 6 93 600	1.8 1.5 23 900	0.45 0.37 5.8 2,200	192 160 17,000 90	48 40 4,220 100	12 10 1,050 140	3 2.5 260 320	rps rps °/s ² msec

Data changes on the leading edge of the CB pulse, and data can be transferred 0.5 μsec after the leading edge.

The simplest method of interfacing with a computer is to transfer data at a fixed time interval after the Inhibit is applied. The converter will ignore an Inhibit during the "busy" interval until that interval is over. Timing is as follows: (a) apply the Inhibit, (b) wait 0.5 μ sec, (c) transfer the data, (d) release the Inhibit. The Inhibit line has no effect on converter tracking.

SIGNAL INPUTS

To prevent damage to the inputs, the maximum steady-state voltage should not exceed the specified input voltage by more than 30%.

ACCOMMODATING NON-STANDARD INPUT VOLTAGES (A ONLY)

The signal and reference input levels can be resistively scaled to accommodate non-standard voltages, see FIGURE 3. Select a converter that is the next lower standard voltage, and the voltage is then scaled up by using resistors in series with the synchro and/or reference inputs.

For a synchro input (SDC), a resistor ${\sf R}_{\sf SIG}\,$ is added in series with S1, S2 and S3 which is determined as follows:

R_{SIG} = 1.1k (New L-L Voltage – Standard Unit L-L Voltage)

That is, 1.1k for each volt above the design voltage level of the standard unit.

Example: An SDC-634A-L (11.8 V) is to be used at 50 V L-L.

 $R_{SIG} = 1.1k (50 - 11.8) = 42.2k$

The closest available high grade resistor with a low temperature coefficient of resistance should be used, and the three resistors should be as closely matched to each other as possible. In general, a 0.1% difference will introduce 1.7 arc minutes of additional error due to the effect on SIN/COS ratio relationship.

The ABSOLUTE value of the resistor is not critical.

In the case of the RESOLVER version (RDC), the equation is:

R_{SIG} = 2.2k (New L-L Voltage – Standard Unit L-L Voltage)

The calculated resistors are connected in series with S1 and S2 respectively. Note only two resistors are required. The required resistance matching and its effect on accuracy, is the same as for a synchro input, see FIGURE 3. The Reference Voltage is treated in the same manner, but the value is not critical.

R_{RFF} = 2.8k (New Reference – Standard Reference)

For this use a 10% tolerance resistor is adequate.

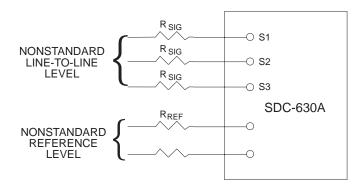
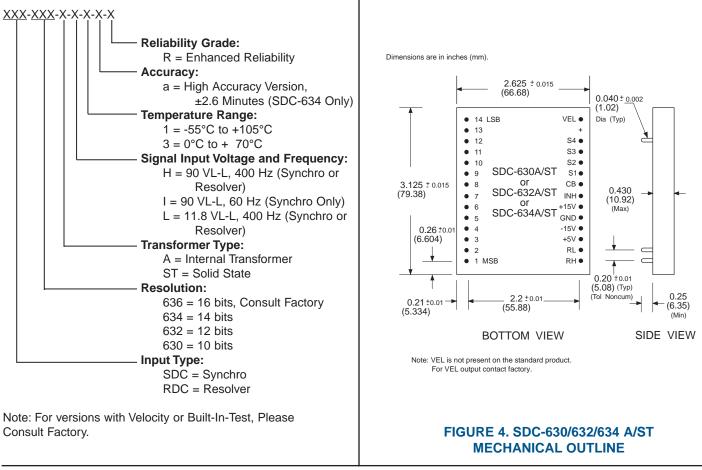


FIGURE 3. SDC-630/632/634 A/ST NON-STANDARD INPUT LEVEL SCALING

ORDERING INFORMATION



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